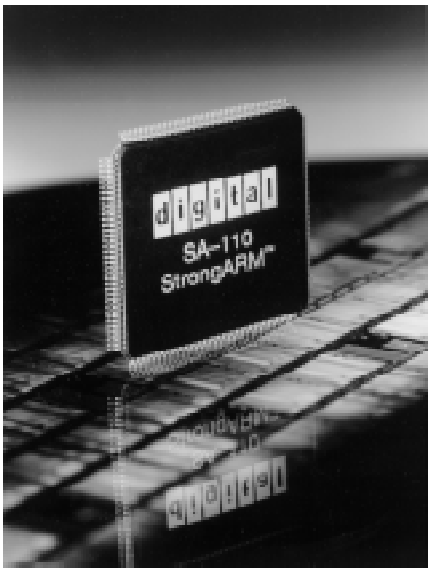
digital

SA-110
StrongARM
166, 200, 233 MHz

Digital Semiconductor SA-110 Microprocessor for Embedded Applications Product Brief



The Digital Semiconductor SA-110 Microprocessor (SA-110), the first member of the StrongARM family of high-performance, low-power microprocessors, is optimized for embedded consumer applications. Featuring superior power efficiency, low cost, and the highest performance and price/performance in the industry, the SA-110 is ideal for high-bandwidth network switching, intelligent office machines, storage systems, and internet appliances. In addition to delivering unparalleled performance in a low-power design, the SA-110 offers compatibility with existing ARM development tools and operating systems.

Applications

- Embedded control
  - Internetworking: routers, bridges, LAN switches
  - Office automation: printers, scanners, copiers
  - Telecommunication: PBX, cellular base station
  - Storage peripherals: drive and RAID controllers
  - PC add-ins: intelligent I/O cards, LAN/WAN
- Net appliances
  - Internet terminals (PCs)
  - Network computers
  - Digital set-top devices
  - Internet television
  - Video kiosks
  - Web phone
  - Video phone

Benefits

- Industry-leading price performance ideal for any consumer product that demands high performance within a tight cost budget.
- Complete suite of software and hardware tools speeds time to market.
- High performance allows DSP function (for example, V. 34 bis soft modem) to be implemented in software, thus reducing system cost.
- Compatibility with ARM and the availability of key third-party development tools (RTOS) reduces design efforts and cost.
- Range of core logic companion chips available (including the Digital Semiconductor 21285 Core Logic).
- Enables manufacturers to compete effectively in the rapidly embedded consumer application market.

Description

The SA-110 is a general-purpose, 32-bit RISC microprocessor with a 16KB instruction cache (Icache); a 16KB write-back data cache (Dcache); a write buffer; and a memory-management unit (MMU) combined in a single chip. The five-stage pipeline distributes tasks evenly over time to remove bottlenecks, ensuring high throughput for the core logic. The SA-110 onchip MMU supports a conventional two-level page-table structure, with a number of extensions. These features result in a high instruction throughput and impressive real-time response for a small and cost-effective chip.

Features

- High performance
  - –192 Dhrystone 2.1 MIPS @ 166 MHz
  - –230 Dhrystone 2.1 MIPS @ 200 MHz
  - –268 Dhrystone 2.1 MIPS @ 233 MHz
- Low power (normal mode)
  - –230 mW @ 2.0-V/166-MHz core/33-MHz bus
  - –330 mW @ 2.0-V/200-MHz core/50-MHz bus
  - –420 mW @ 2.0-V/233-MHz core/66-MHz bus
- Idle and sleep power-down modes
- 32-way set-associative caches
  - –16KB instruction cache
  - –16KB write-back data cache
- 32-entry MMUs
  - –Maps 4KB, 64KB, or 1MB
- Write buffer
  - –8-entry, 16 bytes each
- Memory bus
  - –Asynchronous or synchronous
  - –0-53 MHz @ 166 MHz
  - –0-66 MHz @ 200 MHz
  - –0-66 MHz @ 233 MHz
- Internal phase-locked loop (PLL)
  - –3.68- or 3.56-MHz external reference oscillator
- Big and little endian operating modes
- 3.3-V I/O interface
- 144-pin thin quad flat pack (TQFP)

Microarchitecture

The SA-110 microprocessor is a high-performance implementation of Advanced RISC Machine's ARM Version 4 architecture specification. Figure 1 shows a block diagram of the SA-110.

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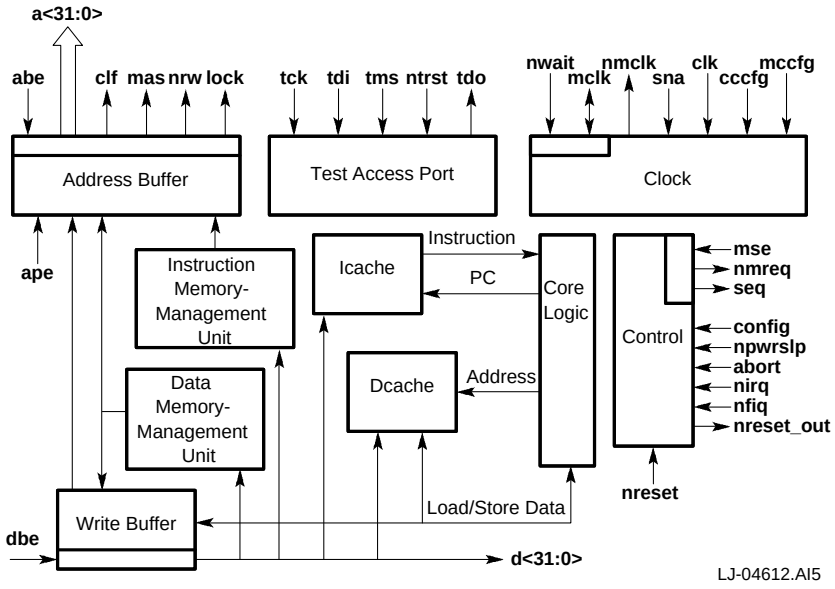
Block Diagram of the SA-110



Bus Interface Logic

The bus interface logic, consisting of the control logic and the address register, controls the bus interface and unplanned events such as interrupts, resets, and aborts. The bus interface logic can also enable or disable wrapping of read transactions and merging of write transactions.

The bus interface can be configured to run synchronously or asynchronously to the core logic. In synchronous mode, the bus interface clock speed is the core clock rate divided by a programmable integer value from 2 to 9 (maximum of 66 MHz).

Write Buffer

The SA-110 has an 8-entry write buffer with each entry able to contain 1 byte to 16 bytes. The write buffer can be enabled or disabled by software. The write buffer is further controlled by a bit in the MMU page tables; so the MMU must be enabled before the write buffer can be used. Software can cause the write buffer to be flushed.

Core Logic

The core logic fetches and executes instructions by using a five-stage pipeline. The five stages are: fetch, decode, arithmetic logic unit (ALU), cache, and write-back. This pipeline arrangement, using the onchip ALU, distributes tasks evenly in time and, therefore, contributes to the high performance of the core logic.

The ARM architecture supports 30 general-purpose registers, 1 program counter, and 6 status registers. There are 16 general-purpose registers (including the PC register) and 1 or 2 status registers visible at any one time. The processor operating mode determines which registers are visible.

The core logic executes the ARM instruction set, which supports straight-forward assembly language code programming. It does not depend upon sophisticated compilers to manage complicated instruction interdependence.

The instruction set has eight instruction classes:

- Two instruction classes use the onchip ALU, barrel shifter, and multiplier to perform high-speed operations on the data in a bank of 16 logical (31 physical) 32-bit registers.
- Three instruction classes control data transfer between memory and the registers. The classes are optimized for flexible addressing, rapid context switching, and swapping data.
- Two instruction classes control execution flow and execution privilege level.
- One instruction class accesses the privileged state of the SA-110.

The core logic implements 32-bit virtual addresses and 32-bit physical addresses. A 12-bit multiplier with early termination performs multiplication. The number of cycles needed to perform a multiplication operation depends on the magnitude of the operands, as shown in Table 1.

Memory-Management Units

The SA-110 has two MMUs: instruction (IMMU) and data (DMMU). Separate translation lookaside buffers (TLBs) are implemented for the instruction and data streams. The TLBs each have 32 entries that can each map a segment, a large page, or a small page. The TLB entry replacement algorithm is round-robin. The data TLB supports both the flush-all and the flush-single-entry function, while the instruction TLB supports only the flush-all function. Memory-management exceptions preserve the base address registers, eliminating the need for "fix-up" code.

Cache

The SA-110 has a 16KB, 32-way, set-associative Icache with 32-byte blocks and a 16KB, 32-way, set-associative, write-back Dcache with 32-byte blocks.

Instruction Cache

The Icache supports the flush-all-entry function, and the replacement algorithm is round-robin within a set. The Icache can be enabled or disabled independent of the memory-management function. When memory management is disabled, the Icache control logic considers all memory to be cacheable.

Data Cache

The write-back Dcache supports the flush-all-entry, flush-entry, and copyback-entry functions. The copyback-all function is not provided in hardware but can be provided by software. The Dcache entries are allocated with read transactions and the entry replacement logic uses a round-robin algorithm.

Clocks

The SA-110 receives a 3.68-MHz clock from a crystal-based clock generator. The SA-110 uses an internal PLL to multiply the frequency by a variable multiplier to produce a high-speed clock. The high-speed clock is then divided internally by a configurable ratio to provide a system clock for synchronous operation. The 3.68-MHz oscillator and PLL run constantly in normal and idle mode.

Boundary-Scan Test Logic

The SA-110 boundary-scan interface provides for driving and sampling of all the external pins of the device except **npwrslp**, irrespective of the core logic state. This ability permits testing of:

- SA-110 electrical connections to the circuit board.
- Integrity of connections between devices having a similar interface on the circuit board.

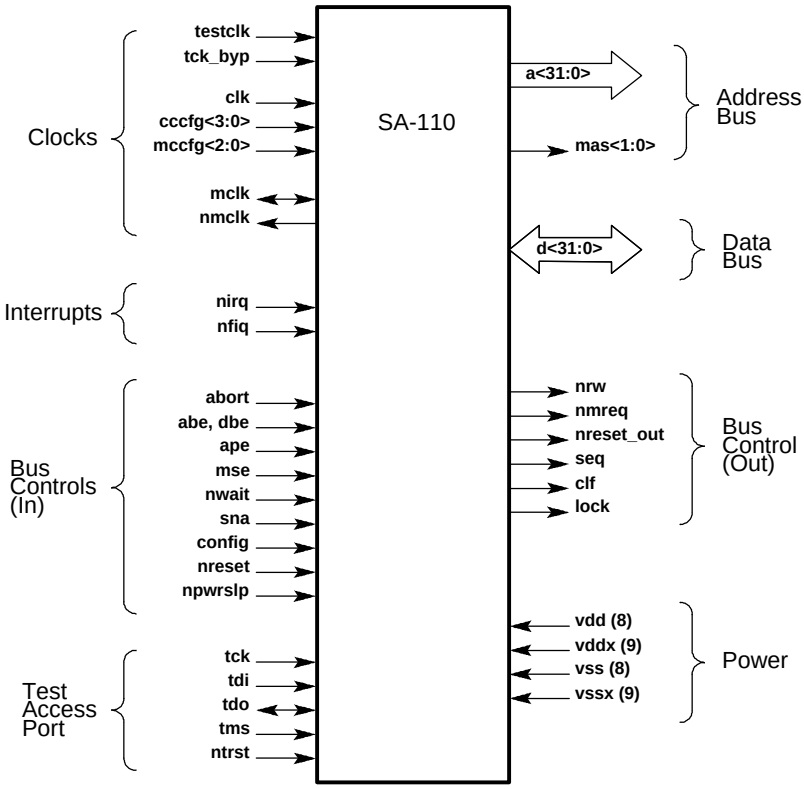
Signal Lines

Figure 2 shows the signal connects to and from the SA-110. The signals are arranged within functional groups.

Core Logic Multiplication Functions

Multiplication Operation (Signed or Unsigned)	Result Size	Operation Duration
32 x 32	32 bits	2–4 cycles
32 x 32 + 32	32 bits	2–4 cycles
32 x 32	64 bits	3–5 cycles
32 x 32 + 64	64 bits	3–5 cycles

Functional Group Signal Lines



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SA-110 Characteristics

	SA-110 166	SA-110 200	SA-110 233
Clock	166 MHz	200 MHz	233 MHz
V2.1 Dhrystone MIPS	192	230	268
Core power supply	**vss** = 0.0 V dc **vdd** = 2.0 V dc ± 10%	**vss** = 0.0 V dc **vdd** = 2.0 V dc ± 10%	**vss** = 0.0 V dc **vdd** = 2.0 V dc ± 5%
I/O power supply	**vddx** = 3.3 V dc ± 10% **vssx** = 0.0 V dc	**vddx** = 3.3 V dc ± 10% **vssx** = 0.0 V dc	**vddx** = 3.3 V dc ± 10% **vssx** = 0.0 V dc
Power dissipation	Maximum = <450 mW	Maximum = <900 mW	Maximum = <1000 mW
Operating temperature	Tj = 100°C (212°F)	Tj = 100°C (212°F)	Tj = 100°C (212°F)
Storage temperature	–40°C to +125°C (–40°F to +257°F)	–40°C to +125°C (–40°F to +257°F)	–40°C to +125°C (–40°F to +257°F)
Packaging Process technology Transistor count Die size	TQFP .35 µm, 3-layer metal 2.1 million 50 mm**2	TQFP .35 µm, 3-layer metal 2.1 million 50 mm**2	TQFP .35 µm, 3-layer metal 2.1 million 50 mm**2
Order number	21281–DA	21281–CA	21281–EA

For More Information

To learn more about the availability of the StrongARM SA-110 Microprocessor, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, visit the Digital Semiconductor World Wide Web Internet site:

http://www.digital.com/semiconductor

or contact the Digital Semiconductor Information Line:

United States and Canada
1–800–332–2717

Outside North America
1–510–490–4753

For technical support contact the Digital Semiconductor Customer Technology Center:

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